**FPD LINK**

**Physical Layer Specification 00.06.03.004**

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# Change Control

|  |  |  |  |
| --- | --- | --- | --- |
| **Version** | **Date** | **Author CDSID** | **Changes / Remark** |
| AA | 6/21/2018 | hkadry | Initial Release |
| AB | 4/1/2019 | hkadry | Renamed Document to FPD LINK  Added FPD LINK IV Differential and Single Ended circuit requirements  Updated signal integrity requirements for FPD LINK III and added signal integrity requirements for FPD LINK IV  Updated layout requirements by changing some shalls to shoulds and adding a signal integrity requirement.  Added CSI-x and LVCMOS guidelines/requirements in both hardware and layout  Moved CM choke to connector nodes for differential topologies  Added current requirement note for ferrites and inductors in POC |
|  |  |  |  |

***Note:***

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# Introduction

## Scope

This document will cover the design requirements for the Texas Instruments FPD LINK LVDS solution. The specification will target the hardware design-using differential (e.g., STP, QTP) and single ended (e.g. Coax) communication topologies. The specification will also address power of data lines (PoDL), but for this application, the power will only be over a coax solution (Power of Coax).

The physical layer design requirements will encompass the circuit level and PCB layout design. This specification will also address the PCB link budget for a robust system. The budget will include the PCB circuit traces, components and board connectors.

The channel requirements for cables can be found in FPD LINK Cable/Connector Channel Specification ref [1].

Attention: Failure to comply with these requirements of this specification by any production intent ECU may result in an inability to communicate on the vehicle network for which the ECU was intended.

## Product Overview

FPD LINK is a point to point high speed/bandwidth digital interface that provides command and control capability.

FPD LINK will be a key enabling technology for vehicle system applications that require high bandwidth with command and control for an enhanced driver experience. An example of these systems are infotainment and digital cameras.

FPD LINK is the bi-directional digital protocol with a forward and back channel that has been chosen for future high quality, high-definition camera driver assist applications.

## Network and Topology

FPD LINK is a SerDes wired point-to-point network operating over an impedance controlled single or differential pair. The connector/cable system are shielded and have a 50Ω single ended characteristic impedance or 100Ω differential characteristic impedance.

The network medium can also transport power (PoDL), but for this specific application power will only be provided when using a single ended cable in this case coax (PoC).

This network can only be point to point and will not consist of other topologies.

## Reference Documents

The requirements of the documents listed in the following table, form a part of this specification. The revision levels shown in the table were the latest at the time this specification was written. In the event of a conflict between the requirements of this specification and the reference documents, the requirements in this specification shall have precedence

|  |  |  |  |
| --- | --- | --- | --- |
|  | Document Number | File Name/Reference | Version |
| **1** | 00.06.01.005 | FPD LINK Cable/Connector Assembly Specification | AA |
| **2** | 00.06.03.401 | FPD LINK Physical Layer Design Verification Checklist | AB |
| **3** | FMC 1278 | Electromagnetic Compatibility Specification for Electrical/Electronic Components and Subsystems | Latest |
| **4** | 00.06.03.002 | Netcom Physical Layer Approved Components List | Latest |
| **5** | - | CSI-x Specification (MIPI Alliance) | Latest |
| **6** | - | USCAR 2 Specification | 6 |

Table 1: Reference Documents

## Definitions, Abbreviations and Acronyms

### Abbreviations

|  |  |
| --- | --- |
| CMC | Common Mode Choke |
| COAX | Coaxial |
| ECU | Electronic Control Unit |
| EMC | Electromagnetic Compatibility |
| FMC | Ford Motor Company |
| FPD LINK | Flat Panel Display (FPD) Link III (TI Devices Trademark) |
| GPIO | General Purpose Input/output |
| I2C | Inter - Integrated Circuit |
| JUTP | Jacketed Unshielded Twisted Pair |
| LVDS | Low Voltage Differential Signal |
| PCB | Printed Circuit Board |
| PLL | Phase Lock Loop |
| PoC | Power over Coax |
| PoDL | Power over Data Line |
| QTP | Quad Twisted Pair |
| SDA/SCL | Serial data/clock line |
| SerDes | Serializer/Deserializer |
| SPP | Shielded Parallel Pair |
| STP | Shielded Twisted Pair |
| UTP | Unshielded Twisted Pair |

Table 2: Abbreviations and Acronyms

### Definitions

|  |  |
| --- | --- |
| Bus | A bus is a collection of one or more wires connecting two or more nodes. Each electronic device is equipped with a specific, standardized electronic interface in order to guarantee compatibility between exchanged binary items of information |
| Characteristic Impedance | The impedance along a transmission line, as a result of wave voltage to current ratio |
| Differential signaling | This is a method used to transmit data using two complimentary signals. |
| Imager | The Imager is the video source. It is connected to an FPD LINK Serializer. The Imager and FPD LINK Serializer can be configured through the back channel. |
| Impedance Discontinuity | The impedance mismatch at a junction in an impedance controlled system |
| Insertion Loss | This defines the amount of signal lost during the journey of a signal from point A to point B. |
| Local Node | Local node is a designator given to the ECU that will provide power to another ECU over the data line, in this application coax (PoC) |
| Remote Node | Remote Node is a designator given to the ECU power by a local node over the data line, in this application coax (PoC) |
| Return Loss | This defines the amount of signal reflected back to the source after encountering an impedance mismatch in the medium. Return loss can contribute to insertion loss if significant |

Table 3: Definitions

# Serializer and Deserializer IC Qualification Requirements

All FMC approved SerDes IC’s shall pass the following qualification requirements. Once the test results are presented and approved by the Netcom team it will be added to the approved component list ref [4]. All SerDes IC changes must be reported to and reviewed by the Ford Netcom team.

## EMC Testing

PL\_FPDLINK\_02\_001

The SerDes IC supplier shall demonstrate conformance to FMC EMC requirements with their SerDes IC laid out on a circuit board following all FMC layout requirements described in this specification. EMC testing shall be conducted to the latest FMC EMC specification ref [3]. The following tests shall be conducted:

* Radiated Emissions
  + RE 310 Radiated Emissions
* Radiated Immunity
  + RI 112 - Bulk Current Injection (BCI), (1-400MHz)
  + RI 130, 150 – Coupled Immunity (Parallel wire test)
  + RI 114 – Radiated Immunity (ALSE/Reverberation Method)
  + RI 115 – Handheld mobile
  + CI 280 - ESD (unpowered test)
* The EMC test setup shall include a serializer and deserializer separated with a ≥1.7m and ≤2m harness in accordance to the EMC specification ref [3].

***Note: All test results must be released to Ford Motor Company and will be kept confidential.***

# FPD LINK Circuit Requirements:

FPD LINK allows two transmission topologies, a 100Ω differential and a 50Ω single ended transmission link. Each topology requires a different link circuit. The following circuit diagrams shall be implemented in order to ensure link robustness. It remains the responsibility of the ECU supplier to ensure that the ECU fully complies with the requirements in this specification.

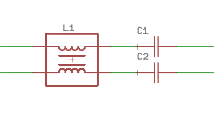
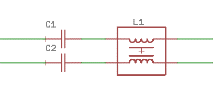
The single ended topology permits providing power over the data link. Furthermore, the FPD LINK chipsets can be configured to use different forward and back channel data rates. Due to these two capabilities, the link circuit and PoC will vary based on the data rate.

The circuits presented in this specification shall be used for all Ford Motor Company modules. The FMC engineer shall review and approve the circuit and PoC used based on the selected chipsets.

## FPD LINK III

### Differential Circuit Topology

PL\_FPDLINK\_03\_001



IC1

SerDes

X1

Board Mounted Connector

X1

Board Mounted Connector

IC2

SerDes

Cable/Connector Assembly

See note (4)

Dout+/Rin+

Dout-/Rin-

Dout+/Rin+

Dout-/Rin-

Figure 1: Differential Pair Circuit

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Ref Des | Type | Value | Tolerance | Current Rating | Voltage Rating | Power Rating(3) | Recommended  Part Number |
| C1(2) | Capacitor | 100nF | ±5% | - | ≥100V | - |  |
| C2(2) | Capacitor | 100nF | ±5% | - | ≥100V | - |  |
| L1(1) | CMC | 90Ω  @100MHz | - | ≥200mA | ≥50V | - |  |
| X1(1) | Board Mounted Connector | - | - | - | - | - |  |
| IC1(1) | IC | - | - | - | - | - |  |
| IC2(1) | IC | - | - | - | - | - |  |

Table 4: FPD LINK III Differential Circuit Parts List

*(1) The components shall be part of the Netcom Physical Layer Approved components list ref [4]*

*(2) Capacitors performance over temperature must be X7R or better.*

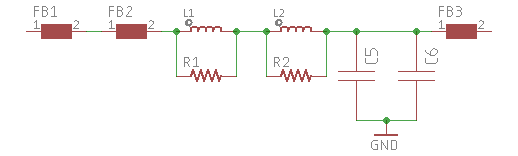
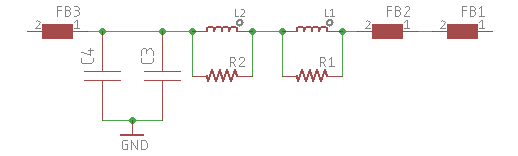
*(3) This is de-rated power based on worst-case circuit analysis for maximum operational temperature of the module*

*(4) The cable/connector assembly requirements and approved parts can be found in the FPD LINK Cable/Connector Assembly Specification ref [1].*

### Single Ended Circuit Topology

#### Single Ended Circuit with Back Channel ≤2.5Mb/s and Forward Channel ≤2.0Gb/s

PL\_FPDLINK\_03\_002

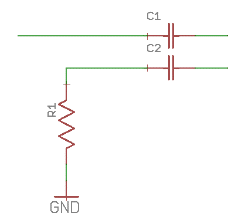
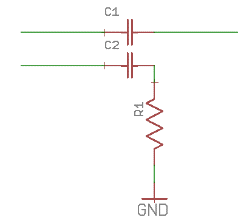


Remote Node

Power Supply

Local Node

Power Supply



IC1

SerDes

X1

Connector

X1

Connector

IC2

SerDes

Cable/Connector Assembly

See note (4)

Dout+/Rin+

Dout-/Rin-

Dout+/Rin+

Dout-/Rin-

Figure 2: Single Ended with PoC Circuit (Back Channel ≤2.5Mb/s, Forward Channel ≤2.0Gb/s)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Ref Des | Type | Value | Tolerance | Current Rating | Voltage Rating | Power Rating(3) | Recommended  Part Number |
| C1(2) | Capacitor | 100nF | ±5% | - | ≥100V | - |  |
| C2(2) | Capacitor | 47nF | ±5% | - | ≥100V | - |  |
| R1 | Resistor | 50Ω | ±0.5% |  |  | ≥50mW |  |
| X1(1) | Board Mounted Connector | - | - | - | - | - |  |
| IC1(1) | IC | - | - | - | - | - |  |
| IC2(1) | IC | - | - | - | - | - |  |

Table 5: Single Ended Circuit Parts List (Back Channel ≤2.5Mb/s, Forward Channel ≤2.0Gb/s)

*(1) The components shall be part of the Netcom Physical Layer Approved components list ref [4]*

*(2) Capacitors performance over temperature must be X7R or better.*

*(3) This is de-rated power based on worst-case circuit analysis for maximum operational temperature of the module*

*(4) The cable/connector assembly requirements and approved parts can be found in the FPD LINK Cable/Connector Assembly Specification ref [1].*

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Ref Des | Type | Value | Tolerance | Current Rating(5) | Voltage Rating | Power Rating(3) | Recommended  Part Number |
| FB1(1) | Ferrite | 1500Ω  @100 MHz | ±10% | Design dependant | - | - | BLM18HE152SH1 |
| FB2(1) | Ferrite | 1500Ω  @100 MHz | ±10% | Design dependant | - | - | BLM18HE152SH1 |
| FB3(1) | Ferrite | 1000Ω  @100 MHz | ±10% | Design dependant | - | - | BLM18AG102SH1 |
| L1(1) | Inductor | 10uH | ±20% | Design dependant | - | - | LQH3NPZ100MGR |
| L2(1) | Inductor | 100uH | ±20% | Design dependant | - | - | CLF6045NIT-101M-D |
| R1 | Resistor | 4.02kΩ | ±1% | - | - | ≥60mW |  |
| R2 | Resistor | 4.02kΩ | ±1% | - | - | ≥60mW |  |
| C3(2) | Capacitor | 100nF | ±20% | - | ≥25V | - |  |
| C4(2) (4) | Capacitor | ≥40uF | ±10% | - | ≥25V | - |  |
| C5(2) | Capacitor | 100nF | ±20% | - | ≥25V | - |  |
| C6(2) (4) | Capacitor | ≥10uF | ±10% | - | ≥25V | - |  |

Table 6: PoC Circuit Parts List (Back Channel ≤2.5Mb/s, Forward Channel ≤2.0Gb/s)

*(1) If the recommended part(s) are not used, alternative part(s) must have same or better performance.*

*(2) Capacitors performance over temperature must be X7R or better.*

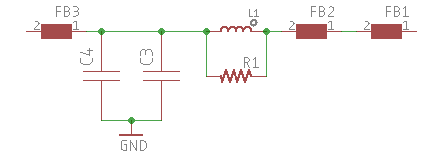
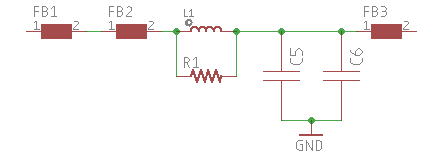
*(3) This is de-rated power based on worst-case circuit analysis for maximum operational temperature of the module*

*(4) The bulk capacitance does not need to be only one capacitor; it can be a combination of multiple parallel caps. However, a decoupling capacitor shall be paired with every bulk capacitor. The total bulk capacitance shall meet the value in the table.*

*(5) This is design dependant based on WCCA anticipated current draw of Remote node*

#### Single Ended Circuit with Back Channel >2.5Mb/s and Forward Channel ≤4.0Gb/s

PL\_FPDLINK\_03\_003

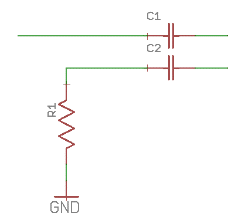
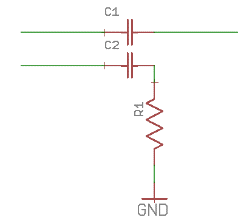


Remote Node

Power Supply

Local Node

Power Supply



IC1

SerDes

X1

Connector

X1

Connector

IC2

SerDes

Cable/Connector Assembly

See note (4)

Dout+/Rin+

Dout-/Rin-

Dout+/Rin+

Dout-/Rin-

Figure 3: Single Ended with PoC Circuit (Back Channel >2.5Mb/s, Forward Channel ≤4.0Gb/s)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Ref Des | Type | Value | Tolerance | Current Rating | Voltage Rating | Power Rating(3) | Recommended  Part Number |
| C1(2) | Capacitor | 33nF | ±5% | - | ≥100V | - |  |
| C2(2) | Capacitor | 15nF | ±5% | - | ≥100V | - |  |
| R1 | Resistor | 50Ω | ±0.5% |  |  | ≥50mW |  |
| X1(1) | Connector | - | - | - | - | - |  |
| IC1(1) | IC | - | - | - | - | - |  |
| IC2(1) | IC | - | - | - | - | - |  |

Table 7: Single Ended Circuit Parts List (Back Channel >2.5Mb/s, Forward Channel ≤4.0Gb/s)

*(1) The components shall be part of the Netcom Physical Layer Approved components list ref [4]*

*(2) Capacitors performance over temperature must be X7R or better.*

*(3) This is de-rated power based on worst-case circuit analysis for maximum operational temperature of the module*

*(4) The cable/connector assembly requirements and approved parts can be found in the FPD LINK Cable/Connector Assembly Specification ref [1].*

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Ref Des | Type | Value | Tolerance | Current Rating(5) | Voltage Rating | Power Rating(3) | Recommended  Part Number |
| FB1(1) | Ferrite | 1500Ω  @100 MHz | ±10% | Design dependant | - | - | BLM18HE152SH1 |
| FB2(1) | Ferrite | 1500Ω  @100 MHz | ±10% | Design dependant | - | - | BLM18HE152SH1 |
| FB3(1) | Ferrite | 1000Ω  @100 MHz | ±10% | Design dependant | - | - | BLM18AG102SH1 |
| L1(1) | Inductor | 10uH | ±20% | Design dependant | - | - | LQH3NPZ100MGR |
| R1 | Resistor | 2kΩ | ±1% | - | - | ≥60mW |  |
| C3(2) | Capacitor | 100nF | ±20% | - | ≥25V | - |  |
| C4(2) (4) | Capacitor | ≥40uF | ±10% | - | ≥25V | - |  |
| C5(2) | Capacitor | 100nF | ±20% | - | ≥25V | - |  |
| C6(2) (4) | Capacitor | ≥10uF | ±10% | - | ≥25V | - |  |

Table 8: PoC Circuit Parts List (Back Channel >2.5Mb/s, Forward Channel ≤4.0Gb/s)

*(1) If the recommended part(s) are not used, alternative part(s) must have same or better performance.*

*(2) Capacitors performance over temperature must be X7R or better.*

*(3) This is de-rated power based on worst-case circuit analysis for maximum operational temperature of the module*

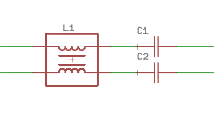
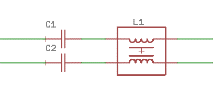
*(4) The bulk capacitance does not need to be only one capacitor; it can be a combination of multiple parallel caps. However, a decoupling capacitor shall be paired with every bulk capacitor. The total bulk capacitance shall meet the value in the table.*

*(5) This is design dependant based on WCCA anticipated current draw of Remote node*

## FPD LINK IV

### Differential Circuit Topology

PL\_FPDLINK\_03\_004



IC1

SerDes

X1

Board Mounted Connector

X1

Board Mounted Connector

IC2

SerDes

Cable/Connector Assembly

See note (4)

Dout+/Rin+

Dout-/Rin-

Dout+/Rin+

Dout-/Rin-

Figure 4: Differential Pair Circuit

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Ref Des | Type | Value | Tolerance | Current Rating(3) | Voltage Rating | Power Rating | Recommended  Part Number |
| C1(2) | Capacitor | 100nF | ±5% | - | ≥100V | - |  |
| C2(2) | Capacitor | 100nF | ±5% | - | ≥100V | - |  |
| L1(1) | CMC | 120Ω  @100MHz | - | ≥200mA | ≥50V | - |  |
| X1(1) | Board Mounted Connector | - | - | - | - | - |  |
| IC1(1) | IC | - | - | - | - | - |  |
| IC2(1) | IC | - | - | - | - | - |  |

Table 9: FPD LINK IV Differential Circuit Parts List

*(1) The components shall be part of the Netcom Physical Layer Approved components list ref [4]*

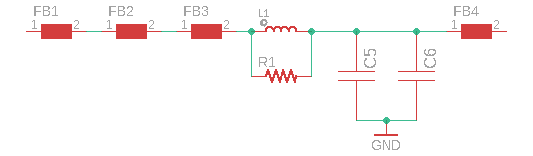
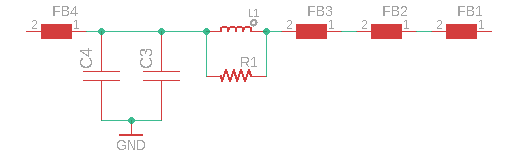
*(2) Capacitors performance over temperature must be X7R or better.*

*(3) This is de-rated power based on worst-case circuit analysis for maximum operational temperature of the module*

*(4) The cable/connector assembly requirements and approved parts can be found in the FPD LINK Cable/Connector Assembly Specification ref [1].*

### Single Ended Circuit with Back Channel >200 Mb/s and Forward Channel 6Gb/s and 8Gb/s

PL\_FPDLINK\_03\_005

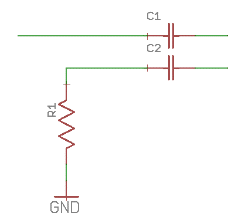
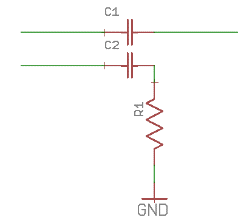


Remote Node

Power Supply

Local Node

Power Supply



IC1

SerDes

X1

Connector

X1

Connector

IC2

SerDes

Cable/Connector Assembly

See note (4)

Dout+/Rin+

Dout-/Rin-

Dout+/Rin+

Dout-/Rin-

Figure 5: FPD LINK IV Single Ended with PoC Circuit (Back Channel >200Mb/s, Forward Channel ≤8.0 Gb/s)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Ref Des | Type | Value | Tolerance | Current Rating | Voltage Rating | Power Rating(3) | Recommended Part Number |
| C1(2) | Capacitor | 100nF | ±5% | - | ≥100V | - |  |
| C2(2) | Capacitor | 47nF | ±5% | - | ≥100V | - |  |
| R1 | Resistor | 50Ω | ±0.5% |  |  | ≥50mW |  |
| X1(1) | Connector | - | - | - | - | - |  |
| IC1(1) | IC | - | - | - | - | - |  |
| IC2(1) | IC | - | - | - | - | - |  |

Table 10: FPD LINK IV Single Ended Circuit Parts List (Back Channel >200Mb/s, Forward Channel ≤8.0Gb/s)

*(1) The components shall be part of the Netcom Physical Layer Approved components list ref [4]*

*(2) Capacitors performance over temperature must be X7R or better.*

*(3) This is de-rated power based on worst-case circuit analysis for maximum operational temperature of the module*

*(4) The cable/connector assembly requirements and approved parts can be found in the FPD LINK Cable/Connector Assembly Specification ref [1].*

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Ref Des | Type | Value | Tolerance | Current Rating(5) | Voltage Rating | Power Rating(3) | Recommended  Part Number |
| FB1(1) | Ferrite | 1500Ω  @100 MHz | ±10% | Design dependant | - | - | BLM18HE152SH1 |
| FB2(1) | Ferrite | 1500Ω  @100 MHz | ±10% | Design dependant | - | - | BLM18HE152SH1 |
| FB3(1) | Ferrite | 1500Ω  @100 MHz | ±10% | Design dependant | - | - | BLM18AG152SH1 |
| FB4(1) | Ferrite | 1000Ω  @100 MHz | ±10% | Design dependant | - | - | BLM18AG102SH1 |
| L1(1) | Inductor | 10uH | ±20% | Design dependant | - | - | LQH3NPZ100MGR |
| R1 | Resistor | 2kΩ | ±1% | - | - | ≥60mW |  |
| C3(2) | Capacitor | 100nF | ±20% | - | ≥25V | - |  |
| C4(2) (4) | Capacitor | ≥40uF | ±10% | - | ≥25V | - |  |
| C5(2) | Capacitor | 100nF | ±20% | - | ≥25V | - |  |
| C6(2) (4) | Capacitor | ≥10uF | ±10% | - | ≥25V | - |  |

Table 11: PoC Circuit Parts List (Back Channel >2.5Mb/s, Forward Channel ≤4.0Gb/s)

*(1) If the recommended part(s) are not used, alternative part(s) must have same or better performance.*

*(2) Capacitors performance over temperature must be X7R or better.*

*(3) This is de-rated power based on worst-case circuit analysis for maximum operational temperature of the module*

*(4) The bulk capacitance does not need to be only one capacitor; it can be a combination of multiple parallel caps. However, a decoupling capacitor shall be paired with every bulk capacitor. The total bulk capacitance shall meet the value in the table.*

*(5) This is design dependant based on WCCA anticipated current draw of Remote node*

# Hardware Design Requirements

PL\_FPDLINK\_04\_001

SerDes IC Power Supply

1. Ferrites shall be used for all SerDes IC input supply pins if recommended by SerDes IC supplier.
2. The smallest value decoupling capacitor as designated by SerDes IC supplier shall be placed as close as possible to designated power supply pins.
3. Sufficient bulk capacitance ≥10uF shall be placed close to the SerDes IC power supply pins.
4. Power strategy shall be reviewed and approved by the IC supplier.

PL\_FPDLINK\_04\_002

Pins

1. Ensure all used pins are configured correctly on the SerDes IC based on the network configuration and SerDes IC supplier design guidelines.
2. If a pin is not being used, then terminate based on chip supplier recommendation. If no recommendation is present: For I/O ports set as output to 0V. For input only ports, terminate with pull-down (Pull down value must be appropriate based on pin current and on/off voltage specification)

PL\_FPDLINK\_04\_003

Crystal/Reference Clock

1. If the Serializer and Deserializer are in Asynchronous mode meaning clock is derived from a local crystal or clock reference:
   1. The crystal shall have a tolerance of ≤50ppm *(This shall include crystal manufacturing tolerance, aging and temperature)*.
   2. Clock jitter requirements must follow the data sheet requirements for each specific chipset.
   3. Crystal load capacitance shall be calculated and selected carefully. Calculation analysis must include board trace and pin input capacitance. Evidence for crystal characterization shall be presented to FMC engineer. This is covered in latest hardware review checklist section 3.2 item 3.2.60. It is recommended to use NP0, COG type capacitors with low ESR for the crystal load capacitance and low inductance resistors for any inline resistors placed on the crystal drive pin.
2. Serializer can utilize synchronous mode meaning they will receive their reference clock over the data link from the remote Deserializer (which follows the Asynchronous requirements above).

PL\_FPDLINK\_04\_004

Reset/Power-Up

1. There is no reset pin available on the chipsets. To reset the chip, the PDB pin must be held low for a specific time. The PDB pin timing must meet the timing requirements detailed in the suppliers latest component data sheet. If a passive circuit is used to set the PDB timing, then an analysis must be performed for a minimum power down time allowed by software. (e.g. RC circuit)
2. Reset/Power-up strategy shall be presented to the FMC engineer for approval.

PL\_FPDLINK\_04\_005

Auto configuration via pin strapping

1. Certain modes can be configured via hardware pin strapping. If the host is not able to configure the part then hardware pin strapping is required. The pin strapping strategy will need to be reviewed by FMC engineer and approved. Pin strapping must be done in accordance to the chipset latest data sheet.

PL\_FPDLINK\_04\_006

CSI-x Interface

1. No components shall be placed on the CSI-x traces.
2. Ensure the recommended slew rate is selected to meet EMC performance.
3. An analysis of signal over-shoot and under-shoot shall be provided for CSI-x signal lines to confirm that IC pin limits are not violated.
4. CSI-x connection are point to point and cannot be daisy chained.

PL\_FPDLINK\_04\_007

I2C interface (This is a mature interface but here are some reminders)

1. The I2C is an open drain interface. The data lines shall each have a pull-up resistor. The value of the resistor is based on the data rate requirements and capacitive loading. Justification shall be provided for the chosen values.
2. If multiple SerDes IC’s are sharing the same I2C, then each SerDes IC shall have a unique address. This is achieved by pin strapping PL\_FPDLINK\_04\_005. Please reference the SerDes IC data sheet to see what pin and strapping mechanism is used.

# Board Layout Design Requirements

PL\_FPDLINK\_05\_001

PCB Stack-up

FMC engineer shall review board stack up. Ensure there is a solid ground reference plane. The reference plane must be adjacent (underneath or above, no layers in between) the high-speed signals.

*Notes:*

*1. Due to the use of inline component(s) on impedance-controlled traces, it is important that a stack-up be selected to allow the component pads to meet the required impedance.*

*2. Ford highly recommends using six layer boards when designing with high speed signals. This allows such signals to be contained on inner layers for optimum EMC performance.*

PL\_FPDLINK\_05\_002

Grounding

All grounding of the system components (SerDes IC, capacitors, chokes, microprocessor, termination, etc.) shall connect to the same ECU ground plane.

PL\_FPDLINK\_05\_003

Ground Plane

An unobstructed ground plane is required on the adjacent layer under all SerDes IC, components and traces.

PL\_FPDLINK\_05\_004

PHY IC Layout

The SerDes IC shall be located close to the edge connector. Other IC’s are not permitted between the connector and the SerDes IC. The maximum distance (trace length, components) from the connector to the IC pins should be ≤2inches (50.8mm)

PL\_FPDLINK\_05\_005

Dout+/Rin+, Dout-/Rin- PCB Characteristics

1. Differential Configuration (The trace pair on the serializer is (Dout+, Dout-) and on the Deserializer is (Rin+, Rin-))
2. (Dout+ / Dout-) and (Rin+ / Rin-) circuit traces between connector and SerDes IC shall be routed as a differential pair and should have a characteristic impedance of 100Ω ±10%. For measured/simulated data, supplier shall use the correct rise time of the signal being sent over the pair. *Faster rise times can be used for an in-depth analysis but may lead to false failures.*
3. The length of (Dout+ / Dout-) and (Rin+ / Rin-) circuit traces from the connector pins to the SerDes IC pins should be symmetrical to each other (mirror copies of one another, trace length matching ±10mils).
4. Single Ended Configuration
5. For the single ended configuration, Dout+ and Rin+ shall be routed as a single ended and should have an impedance of 50Ω ±10%. Since the chip is still considered differential, there are two options for routing Dout- /Rin-.
   1. If ≥ 3x(x=trace width) spacing between Dout+ Dout- and between Rin+ Rin- can’t be guaranteed while routing, then Dout- and Rin- should be terminated at the SerDes IC pin and Dout+ and Rin+ shall be routed alone.
   2. If ≥3x (x=trace width) spacing between Dout+ Dout- and between Rin+ Rin- can be guaranteed, then Dout- can be routed along with Dout+ and Rin- can be routed with Rin+ as single ended 50Ω ±10% and terminated as close as possible to the connector.

PL\_FPDLINK\_05\_006

Connector Characteristics

1. The connector is designed to have differential impedance of 100Ω±10% or single ended impedance of 50Ω±10%. However, the connector footprint (surface mount, through hole) might behave differently based on the PCB stack up. The supplier shall perform the following to ensure a robust design.
   1. For a surface mount connector, ensure the landing pad is impedance controlled by referencing the correct ground plane. Copper planes (ground, power and signal) should be removed underneath the landing pad to meet the impedance requirements.
   2. For a through-hole connector, the connector pin(s) drill size is specified by the connector supplier, however based on the PCB stack up the anti-pad will vary to control the impedance going into the board. If possible, route on the outermost layer opposite to the connector to avoid having a stub created by the connector pin. The module supplier must provide a simulation of the connector with the module PCB stack up to ensure the correct footprint is implemented for impedance control. This analysis can be conducted with the connector supplier.
2. The connector footprint must meet the soldering requirements as defined by the circuit board assembly process. Pin in paste applications must show that sufficient solder volume is available to fill the through hole. This analysis can be conducted with the connector supplier and the PCB manufacturing facility.

PL\_FPDLINK\_05\_007

Components

In-line components (e.g. capacitors, inductors, resistors), connector footprint, and IC pin pads should have minimal effect ±10% on the characteristic impedance.

* 1. Based on the component pad size (e.g., capacitor, inductor, resistor, IC pins), the reference plane directly underneath the component might restrict the component’s pad(s) from being impedance matched. To control the impedance the supplier should determine the correct reference plane and remove all metal on all planes before the determined reference plane.
  2. For ‘T’ connection components, there should be no stub trace or via. The pad of the first component should be in series with the trace. The pad should also be impedance matched and follow the design requirements in part ‘1’ above. (E.g. first component of POC, termination circuit, etc.)

PL\_FPDLINK\_05\_008

High Speed Differential/Single Ended Signals

1. High-speed differential/single ended signals should be routed with ≤ 3 vias and should maintain their characteristic impedance from start to finish.
2. If transitions are necessary, a ground via shall be placed at the transition point via. For differential traces via transitions shall be symmetric.
3. If high-speed signals are transitioned to an inner layer, it is recommended keep routing on same layer and transition back at IC connection point. This will keep the high-speed trace buried between two planes.
4. High-speed signals shall not be routed over any ground/power plane splits. All high speed/controlled signals shall be routed with reference plane above or below them.
5. If test points are needed, they should be placed in series with routing to avoid creating a stub. Differential pair test points should be symmetrical and in the same location.
6. 90-degree bends shall not be used on traces. Use 45-degree bends to give an angle ≥135°.
7. Separation distance between differential and single ended signals
   1. There should be ≥2x (x=differential pair separation) separation between adjacent sets of high-speed differential signal pairs
   2. There should be ≥2x (x=single ended trace width) between single ended signals
   3. There should be ≥3x (x=differential pair separation) between a differential pair and single ended signal.
8. Inline capacitors should be symmetrical on a differential pair
9. Inline capacitors should not be aligned on adjacent non-differential high-speed signals.

PL\_FPDLINK\_05\_009

Crystal PCB Layout

FMC engineer shall review and approve the crystal layout. Crystal supplier shall perform a layout review.

1. Crystal components should be placed as close as possible to the XTAL and EXTAL pins to minimize routing distances.
2. No other signals shall be routed over the crystal circuit without an intervening reference plane in between.
3. Crystal XTAL/EXTAL traces should be routed on the same layer. Transitions are not recommended.
4. Multiple vias should be used when connecting crystal pins/components to a ground plane.

PL\_FPDLINK\_05\_010

Reference Clock PCB Layout

Reference clock traces shall be impedance controlled and matched to the IC termination impedance within ±10% Reference clock traces shall be ≥20x (x=trace width) from the edge of the boards and ≥3x from surrounding signal traces.

PL\_FPDLINK\_05\_011

Magnetic Component Separation

When multiple FPD LINK channels are routed on the same board, link components (e.g. CMC, Noise Filters, etc.) Shall have a separation distance of ≥2mm.

PL\_FPDLINK\_05\_012

Multi-Link Separation and Isolation

If multiple FPD LINK circuits exist on the same PCB, then link routing shall have a separation of ≥3x between pairs. (x=differential pair separation, single ended trace width).

PL\_FPDLINK\_05\_013

CSI-x Signal Lines

All CSI-x signals shall be routed differentially with the following requirements

1. Flight time shall be ≤2ns
2. Traces should be symmetrical to each other (mirror copies of one another, trace length matching ±1%)
3. In high power mode only, the signals can be loosely or tightly coupled and should have a

100Ω±10% differential impedance

1. In lower power mode only , the signals should be loosely coupled ≥3x (x=trace width) and shall have a 50Ω±10% single ended impedance
2. If both high and low power modes are used, the signals should be loosely coupled ≥3x (x=trace width) and should have a 50Ω±10% single ended impedance and a 100Ω±10% differential impedance.
3. Supplier must provide signal integrity analysis for FMC review.
   1. The analysis shall show a return loss ≤ -13dB at the operating frequency
   2. The analysis shall show an insertion loss ≤2dB at the operating frequency
   3. The analysis shall show a crosstalk isolation of 30dB or better from surrounding signals. If 30dB of isolation cannot be met then an analysis of the signal characteristics of the victim trace must show that the signal integrity is maintained in the presence of the crosstalk.

PL\_FPDLINK\_05\_013

Parallel Data Signal Lines (LVCMOS)

All parallel data signals shall be routed single ended with the following requirements

1. All single ended lines should be electrically matched ±1%.
2. The signals should be loosely coupled ≥2x (x=trace width) and shall have a 50Ω±10% single ended impedance
3. Supplier must provide signal integrity analysis for FMC review.
   1. The analysis shall show a return loss ≤ -13dB at the operating frequency
   2. The analysis shall show an insertion loss ≤2dB at the operating frequency
   3. The analysis shall show a crosstalk isolation of 30dB or better from surrounding signals. If 30dB of isolation cannot be met then an analysis of the signal characteristics of the victim trace must show that the signal integrity is maintained in the presence of the crosstalk.

# SerDes PCB Circuit S-Parameter Requirements

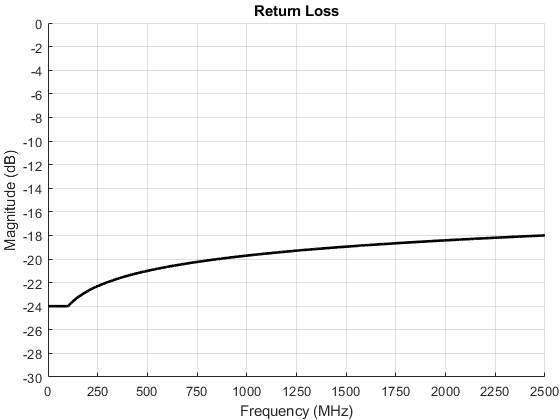
The FPD LINK SerDes circuit *(PCB differential or Single ended traces* (Dout+/Rin+) & (Dout-/Rin-)*, CMC, capacitors, PoC, AC termination and board header connector, SerDes IC pads etc.)* reference circuit figures of Section 3 shall meet the signal integrity limit lines presented in this section.

Signal integrity simulations for the circuit are permitted as proof of compliance to pass ref [2]. However, if PCB is available prior to FDJ, circuit signal integrity measurement data shall also be provided. Supplier must also show evidence that PCB signal integrity measurement data will be captured on their final PCB design. Testing should be done during their DVP but must be completed in PVP. Measurements or simulations shall consider all PCB manufacturing tolerances.

## FPD LINK III

### Return Loss (sdd11, sdd22, s11, s22)

PL\_FPDLINK\_06\_001



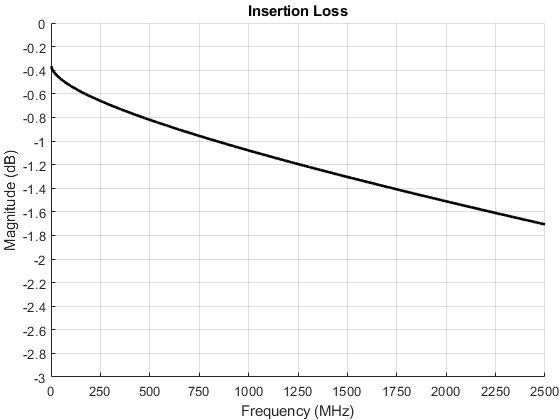
PASS

FAIL

Figure 6: FPD LINK III PCB Return Loss Limit

### Insertion Loss (sdd12, sdd21, s12, s21)

PL\_FPDLINK\_06\_002



PASS

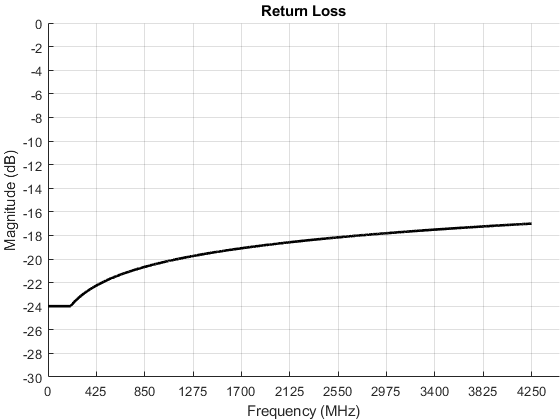
FAIL

Figure 7: FPD LINK III PCB Insertion Loss Limit

## FPD LINK IV

### Return Loss (sdd11, sdd22, s11, s22)

PL\_FPDLINK\_06\_003



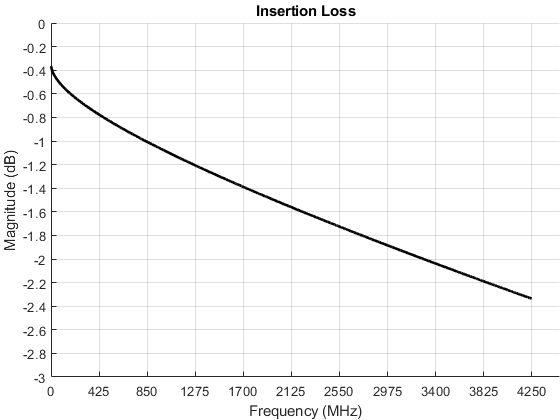
FAIL

PASS

Figure 8: FPD LINK IV PCB Return Loss Limit

### Insertion Loss (sdd12, sdd21, s12, s21)

PL\_FPDLINK\_06\_004



FAIL

PASS

Figure 9: FPD LINK IV PCB Insertion Loss Limit

## PoC Impedance Characteristics

PL\_FPDLINK\_06\_005

Supplier shall perform Impedance vs. Frequency analysis, unloaded and load max current on the PoC from the backchannel frequency to the forward channel frequency and present impedance data to FMC engineer. Supplier must determine impedance requirement from IC supplier.

(E.g. 933/934 ≥1kΩ, 953/954 ≥2kΩ)

# Verification Method

|  |  |
| --- | --- |
| **Protocol** | **Conformance Test** |
| FPD LINK | All PL\_FPDLINK requirements will be reviewed in the FPD LINK Physical Layer Design Verification Checklist ref[2] |
|  |  |
|  |  |

Table 12: Document Verification Table